WHAT IS CLAIMED IS:

1. A content addressable memory (CAM) cell comprising:

a memory cell operable to store a bit value; and

a comparison circuit coupled to the memory cell and configured to detect the bit value stored in the memory cell, the comparison circuit including

the output transistors coupled to a match line and configured to provide a logic comparison between the stored bit and the input bit as well as drive for the match line based on the result of comparison , and

the dummy transistors coupled to a dummy line, wherein the match line and dummy line are used to detect an output value provided by the CAM cell.

2. The CAM cell of claim 1, wherein the dummy transistors has same dimension as the output transistors and are located in close proximity to the transistors driving the match line .

3. The CAM cell of claim 1, wherein the dummy transistor is turned OFF during sensing operation.

4. A Ternary content addressable memory (CAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a few pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a few pairs of dummy transistors coupled to a dummy line, wherein the match line and dummy line are used to detect an output value provided by the CAM cell.

5. The CAM cell of claim 4, wherein the dummy transistors have similar dimension as the output transistors and are located in close proximity to the output transistors.

6. The CAM cell of claim 4, wherein the dummy transistors are turned OFF during sensing operation.

7. A dummy content addressable memory (CAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a pair of dummy transistors coupled to a dummy line and configured to provide a drive for the dummy line based on an inverted detected data bit value and the detected control bit value.

8. The DUMMY CAM cell of claim 7, wherein the comparison circuit further includes the transistors connected to the dummy line has half the driving capability as those transistors connected to the match line